(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: 0 575 854 A2

(12) EUROPEAN PATENT APPLICATION

(21) Application number: 93109483.3

(51) Int. Cl.5: G05B 23/02

(22) Date of filing: 14.06.93

(30) Priority: 17.06.92 JP 157907/92

(43) Date of publication of application:
29.12.93 Bulletin 93/52

(84) Designated Contracting States:
DE GB

(71) Applicant: Sumitomo Electric Industries, Ltd.
5-33, Kitahama 4-chome, Chuo-ku
Osaka 541(JP)

(72) Inventor: Hashiba, Hitoshi, c/o Osaka Works of Sumitomo
Elec. Ind. Ltd
1-3, Shimaya 1-chome
Konohana-ku, Osaka(JP)
Inventor: Isshiki, Isao, c/o Osaka Works of Sumitomo
Elec. Ind. Ltd
1-3, Shimaya 1-chome
Konohana-ku, Osaka(JP)
Inventor: Makino, Fumio, c/o Osaka Works of Sumitomo
Elec. Ind. Ltd
1-3, Shimaya 1-chome
Konohana-ku, Osaka(JP)
Inventor: Nakai, Yoshiharu, c/o Osaka Works of Sumitomo
Elec. Ind. Ltd
1-3, Shimaya 1-chome
Konohana-ku, Osaka(JP)
Inventor: Ueda, Seiji, c/o Osaka Works of Sumitomo
Elec. Ind. Ltd
1-3, Shimaya 1-chome
Konohana-ku, Osaka(JP)

(74) Representative: Schieschke, Klaus, Dipl.-Ing.
Patentanwälte Dipl.-Ing. E. Eder
Dipl.-Ing. K. Schieschke
Elisabethstrasse 34
D-80796 München (DE)

(54) Mutual monitoring circuit for computers.

(57) Mutual monitoring circuits for monitoring any abnormality of a plurality of microcomputers in a control circuit controlled thereby. Monitoring circuits are provided in two microcomputers, respectively, to monitor any abnormal behavior of their counterparts. Each mutual monitoring circuit has a judging unit for giving judgement on whether or not there is abnormality by measuring the pulse frequency and duty of the pulse signals and for outputting abnormality judgement signals upon detecting any abnormality. The judgement signals are sent directly to an input signal line in a driving circuit of a failsafe relay as a load shut-off mechanism, thereby changing its abnormality signals to a low level. This in turn stops the output of the driving circuit, thus shutting off the failsafe relay.

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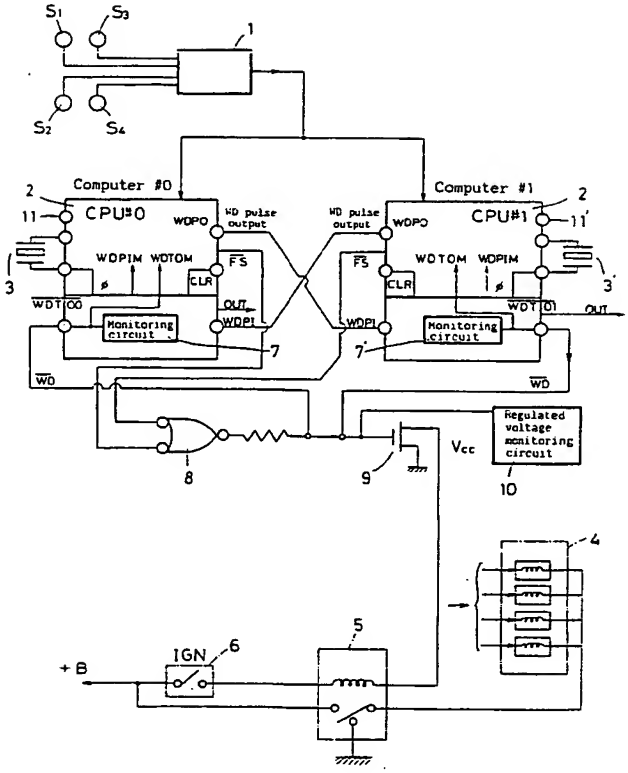
FIG. 1



This invention relates to a monitoring control circuit for monitoring a plurality of computers, more specifically for detecting any malfunctions or runaway of computer for controlling antilock brake system (ABS) for an automobile adapted to prevent locking of the wheels of the automobile by adjusting the pressure of brake fluid when applying a quick brake or the brake on a slippery road, thereby monitoring the system in a normal state.

An electric control circuit of ABS calculates wheel speeds and slip rates in a computer on the basis of information from wheel speed sensors mounted near the wheels and controls, based on the results of calculation, the hydraulic unit which adjusts the pressure of brake fluid more efficiently. Various types of such circuits are known.

Such an electric control circuit of ABS plays an important role of controlling the hydraulic unit, high safety and absolute reliability are essential requirements. Most typically, such a circuit includes at least two microcomputers provided parallel to each other and arranged so as to monitor each other.

An electric control circuit of ABS shown in Fig. 2 by way of example has two microcomputers MC_0 and MC_1 (#0, #1). Wheel speed information supplied from wheel speed sensors S1 - S4 is branched in parallel in the form of pulse signals through an input processing circuit D and inputted in the respective computers. The computers perform arithmetic operations based on the input signals according to a predetermined program and give output signals OUT based on the results of arithmetic operations. These output signals are supplied to solenoid valves or the like as loads to control the braking pressure in the hydraulic line.

During normal and antilock control operations by the microcomputers, watchdog pulse signals WDP_0 and WDP_1 outputted from the two microcomputers MC_0 and MC_1 are inputted in a watchdog circuit WDC to monitor these signals and thus monitor any abnormality of the computers. In the watchdog circuit WDC, the watchdog pulse signals are compared and judgement is made. As far as the two microcomputers are both normal, judgement signals WD are outputted.

Also there is a monitoring circuit HWC for monitoring regulated voltage that is a power supply of the microcomputers. As far as the voltage is normal, that is, lower than a predetermined value, HW is outputted. The WD signals and HW signals are sent through an AND_1 gate to another gate AND_2.

Besides the above monitoring signals, failsafe signals FS_0 and FS_1 are outputted from the respective microcomputers MC_0 and MC_1. The signals will turn to an L0 output if any abnormal behavior is detected during normal and antilock control operations. These signals are sent to the AND_2 gate. If the abovesaid signals are all normal, the AND_2 gate outputs signals to actuate a driving circuit FET and to activate a failsafe relay FSR. In this state, solenoid valve and a motor relay having loads X are in operative condition. Thus, if any one of the input signals to the AND_2 gate turns out to be abnormal, the failsafe relay FSR is cut off so that the antilock controlling is inhibited.

In a known method, if watchdog pulse signals from a main to sub-microcomputer are normal, the main one controls the loads X and if not, the loads X are deactivated by operating the failsafe relay immediately. In other method, the two microcomputers are treated equally. They monitor each other in detail. And if their calculated value such as acceleration, deceleration and vehicle speed is not identical, the loads X are deactivated by operating the failsafe relay. There is a watchdog timer circuit outside the microcomputers which monitor the watchdog pulse signals from the microcomputers. If the watchdog pulse signals are abnormal, the loads X are deactivated by operating the failsafe relay immediately.

In such a conventional monitoring circuit for monitoring the behavior of microcomputers, the normal watchdog pulse signals from the respective microcomputers are given to the watchdog circuit as far as the microcomputers are normal. A watchdog timer is triggered at predetermined time intervals.

Thus, if one of the microcomputers should malfunction and stop producing output signals or produce output signals having abnormal pulse widths, the watchdog timer will not be triggered, so that malfunction of the microcomputer is detectable.

But since such a conventional monitoring circuit using a watchdog timer is provided outside the microcomputers, if the microcomputers used are general-purpose ones, there will arise the problem of layout of parts in designing the circuit, that is, the problem of installation space. Further, the use of gate arrays or linear IC's will push up the cost.

An object of this invention is to provide mutual monitoring circuits which are free of the above-described problems and, which are mounted in the respective microcomputers to monitor watchdog pulse signals mutually and output abnormality judgement signals, if one or some of the microcomputers are found out to be abnormal, to actuate a load shut-off mechanism immediately, and which are simple in structure and less expensive and can cope with any runaway state and thus are highly reliable.

The present invention provides an electronic control circuit having a plurality of microcomputers which operate by mutually independent oscillating sources, wherein input signals such as speed information are divided and inputted in the respective

microcomputers, the microcomputers performing arithmetic operations according to a predetermined program based on the input signals, the electronic control circuit giving output control signals based on the results of the arithmetic operations; a mutual monitoring circuit for monitoring the plurality of microcomputers, a monitoring circuit provided in the each microcomputer and being operative without any software for monitoring the other microcomputer, the one microcomputer sending watchdog signals to the monitoring circuit of the other microcomputer; a judgement unit provided in the monitoring circuit and receiving watchdog signals from the other microcomputer and judging whether the microcomputer is normal or not, and; a load shut-off means receiving the result of judgement and shutting off a load to be controlled if judged abnormal.

In this case, the judgment units can preferably judge the pulse width and duty of the watchdog signals.

Also, an input signal line of the load shut-off mechanism may be a negative-logic AND circuit and the signals from the judgement unit may be applied to the AND circuit, thereby shutting off the load with the load shut-off mechanism if the result of AND operation is abnormal.

Further, though each judgement unit outputs an abnormal judgement signal as soon as it detects any abnormality, it may output a normal judgement signal when the other microcomputer returns to normal only after detecting a predetermined number of normal signals continuously or after detecting normal pulse signals continuous during a predetermined time.

Further, each microcomputer preferably has a monitoring circuit which judges whether other microcomputer is normal or not.

Otherwise, after turning power on and releasing resetting in the electronic control circuit, an initial test is performed in which the watchdog pulse signals produced by the each microcomputer are converted deliberately into abnormal signals and sent to the monitoring circuit in the other microcomputer to check the monitoring function of the respective monitoring circuits.

Also, each microcomputer may have its specific external terminal set at High or Low whereby each microcomputer can be set in a mode wherein the oscillation of quartz oscillators cannot be stopped by software.

According to this invention, if one or some of the microcomputers malfunctions or gets into an abnormal state, the mutual monitoring circuits detect such abnormal state and send judgement signals to the load shut-off mechanism to shut off the load.

Similarly, if all the microcomputers should fail, they can be mutually monitored by means of the monitoring circuits which are contained therein and operate without interposing software. Further, since the oscillation of the quartz oscillators cannot be stopped with software, it is possible to detect any abnormal state reliably and send judgement signals to the load shut-off mechanism to shut off the load.

The input signal line of the load shut-off mechanism is a negative-logic AND circuit. If any one of the abnormality judgement signals such as those representing abnormal in response to watchdog pulses or an abnormal signal as to regulated voltage that is a power supply of the microcomputers is inputted, the load shut-off mechanism is activated, thus shutting off the load.

After turning power on and releasing resetting, watchdog pulse signals produced by one computer are converted deliberately into abnormal signals in various patterns and transmitted to the monitoring circuit in the other computer to check the monitoring function of the respective monitoring circuits. The loads are actually shut off by some of the patterns and the monitoring circuit monitors this fact. But with most other patterns, the monitoring function can be electrically checked at high speed by monitoring the results of judgement on their own without being limited by the mechanically determined time for shutoff and connection of the loads.

The mutual monitoring circuits according to the present invention are extremely simple in structure and thus can be manufactured at low cost. Still, they can respond to any abnormal state in the most appropriate manner and are highly reliable.

Also, since the checking of monitoring function is carried out electrically after turning power on and releasing resetting, checking can be done at high speed.

Other features and objects of the present invention will become apparent from the following description made with reference to the accompanying drawings, in which:

Fig. 1 is a block diagram showing the monitoring circuit according to the present invention; and

Fig. 2 is a block diagram showing a conventional monitoring circuit.

Fig. 1 shows one example of the electronic control circuit of the embodiment and is an entire block diagram including an electric control circuit of ABS and its monitoring circuit. The signals that represent wheel speed information from wheel speed sensors S1 - S4 are converted into pulse signals in a digitalizing circuit 1. They are then split into two lines and read by two independent microcomputers 2, 2'.

The two microcomputers 2, 2' operate on independent reference time periods given by refer-

ence oscillators 3 and 3'. In the embodiment, each computer contains a predetermined program for calculating wheel speeds and slip rates based on the wheel speed information and is provided with a memory for storing these data and information.

The output signals OUT of the microcomputers 2 and 2', which are the results of the calculations, are transmitted to loads such as solenoid valves 4 through e.g. the above-described output determining logic circuit (not shown). The solenoid valves 4 are connected to an unillustrated power supply battery through a contact of a failsafe relay 5. By turning the failsafe relay 5 ON, the solenoid valves 4 are ready ON-OFF control.

The mutual monitoring circuit has the following structure. The microcomputers 2, 2' are provided with monitoring circuits 7, 7', respectively, for monitoring the watchdog pulse signals produced by their respective counterparts. The monitoring circuits 7, 7' are a kind of watchdog timer circuits which operate independently of the software forming a program for antilock control.

The monitoring circuits may comprise watchdog timers having the function of e.g. retriggerable one-shot multivibrators or a similar function. The watchdog timers can measure the number and frequency of the watchdog pulses and detect both long-term and short-term abnormalities. The frequency of the watchdog pulses produced by each microcomputer is set, in a normal state, at a 50% duty ratio. The monitoring circuit has watchdog timers as judgement units which determine whether or not the frequency and duty of the pulse signals are normal. When the pulse signals are inputted as trigger signals, judgement on the frequency and duty is made in the judgement units. If it is judged that the microcomputer is functioning normally, a signal H is produced continuously. If judged abnormal, a signal L is produced.

As soon as one of the judgement units detects any abnormality, it produces abnormality judgement signals. But when the microcomputer on the other side returns to a normal state, the judgement unit will produce a normal judgement output after detecting a predetermined number of normal watchdog pulses or after detecting normal pulse signals continuous during a predetermined time.

Further, electric control circuit of ABS has a so-called self diagnosis function that each microcomputer monitors all of input and output signals so that it can find out any abnormality of its own system. And if either of microcomputers detects any abnormality of the system, it outputs a failsafe signal which is applied to an input signal of AND gate 8.

Its output signals are applied to an FET of a driving circuit 9 as gate signals. Upon receipt of the gate signals, the driving circuit 9 drives the failsafe relay 5 to put the solenoid valves 4 and a motor relay in an operative state.

Connections are made as shown in Fig. 1. A signal from the AND gate 8 to driving circuit 9 is representing abnormality judged from the above-described self-diagnosis of microcomputers. And wires or lines from WD signals of each microcomputer to driving circuit 9 are representing abnormality of either or both of microcomputers judged from mutual monitoring circuits 7, 7' which are mounted in the microcomputers. Also the output of a regulated voltage monitoring circuit 10 is connected to driving circuit 9. It is representing that regulated voltage which is a power supply of microcomputers is higher than predetermined value regarded as normal.

The two microcomputers 2, 2' have the function of monitoring, on their own, the results of judgement as to whether or not the programs in the normal and antilock control circuits are operating normally. This monitoring function in each computer is as follows: After switching on the ignition to turn the power on and releasing resetting, watchdog pulse signals produced by one computer are fed into the other computer after deliberately turning them into abnormal signals by means of a program for initial testing contained in the first computer; the second computer judges and monitors, on its own, the combination pattern of the abnormal and normal signals; and if the combination pattern coincides with a predetermined pattern, the second computer determines that its own monitoring function is normal. One bit in the register in each microcomputer is used for the judgement. If its function is abnormal, the signal fed to the one bit is checked and judged by a soft program.

Also, in order that the microcomputers can be used for general purposes, they are ordinarily provided with a stop mode or a halt mode. By applying special commands, i.e. by a soft program, the crystal oscillator can be stopped from oscillating. Thus, if the software should go uncontrollable, the oscillator might stop oscillating.

But according to this invention, in order to ensure high reliability, each microcomputer is provided with a specific external terminal 11. By setting the external terminal 11 at Hi or Lo, the oscillation stopping function with software is deleted. Namely, by setting the external terminal 11, the crystal oscillating circuit in each microcomputer operates solely on hardware.

The two microcomputers are monitored by the above-described monitoring circuit to see if they are operating normally in the following manner.

For the antilock control, the two microcomputers operate basically in the same way as conventional computers. Thus, no detailed description is made.

As far as there appears nothing abnormal during normal and antilock control operations, the two microcomputers 2, 2' both produce H signals as failsafe relay signals FS_0, FS_1, so that the AND gate 8 gives the H signal, to the gate of the driving circuit 9, thus turning the failsafe relay 5 ON. The AND gate 8 operates on the negative logic.

On the other hand, the mutual monitoring circuits 7, 7' monitor the two microcomputers to see if they are operating normally. The watchdog pulse signals as reference signals of one of the microcomputers are fed to the other microcomputer and checked by the mutual monitoring circuit in the latter computer. If it turns out that both microcomputers are operating normally, a signal H as a judgement signal is produced and given to the gate signal line of the driving circuit 9 as described above. Also, if there is no abnormality in the regulated voltage, a signal H is given to the gate signal line from the regulated voltage monitoring unit 10.

But if any one of the three kinds of monitoring signals turns out to be abnormal, for example, if the failsafe signal FS turns to L, the output of the AND gate 8 will also turn to L, so that the gate signal line of the driving circuit 9 will also turn to L even if the other signals are H. As a result, the failsafe relay 5 is cut. The same happens if the watchdog signal WD or the regulated voltage monitoring signal turns to L.

Thus, according to the above-described logic control, monitoring is carried out not only for the control operations by the two microcomputers but also for any abnormal behavior of the microcomputers themselves. Provided outside the computers is only a gate driving circuit having a simple structure.

Claims

1. In an electronic control circuit having a plurality of microcomputers which operate by mutually independent oscillating sources, wherein input signals such as speed information are divided and inputted in said respective microcomputers, said microcomputers performing arithmetic operations according to a predetermined program based on said input signals, the electronic control circuit giving output control signals based on the results of the arithmetic operations; a mutual monitoring circuit for monitoring said plurality of microcomputers, a monitoring circuit provided in said each microcomputer and being operative without any software for monitoring the other microcomputer, said one microcomputer sending watchdog signals to said monitoring circuit of the other microcomputer; a judgement unit provided in said monitoring circuit and receiving watchdog signals from the other microcomputer and judging whether the microcomputer is normal or not, and; a load shut-off means receiving the result of judgement and shutting off a load to be controlled if judged abnormal.

2. A mutual monitoring circuit as claimed in claim 1 wherein said judgement unit determines whether the pulse width and duty of the watchdog signals are normal or not.

3. A mutual monitoring circuit as claimed in claim 1 or 2 wherein an input signal line of said load shut-off means is a negative-logic AND circuit and wherein the signals from said judgement unit are given to said AND circuit, thereby shutting off the load with said load shut-off means if the result of AND operation is abnormal.

4. A mutual monitoring circuit as claimed in any of claims 1-3 wherein though it outputs an abnormal judgement signal as soon as said judgement unit detects any abnormality, it outputs a normal judgement signal when the other microcomputer returns to normal after detecting a predetermined number of normal pulse signals continuously or after detecting normal pulse signals continuous during a predetermined time.

5. A mutual monitoring circuit as claimed in any of claims 1-4 wherein said each microcomputer has a monitoring circuit which judges whether other microcomputer is normal or not.

6. A mutual monitoring circuit as claimed in any of claims 1-5 wherein after turning power on and releasing resetting in said electronic control circuit, an initial test is performed in which the watchdog pulse signals produced by said each microcomputer are converted deliberately into abnormal signals and sent to said monitoring circuit in the other microcomputer to check the monitoring function of the respective monitoring circuits.

7. A mutual monitoring circuit as claimed in any of claims 1-6 wherein said each microcomputer has its specific external terminal set at High or Low whereby said each microcomputer can be set in a mode wherein the oscillation of quartz oscillators cannot be stopped by software.

FIG. 1

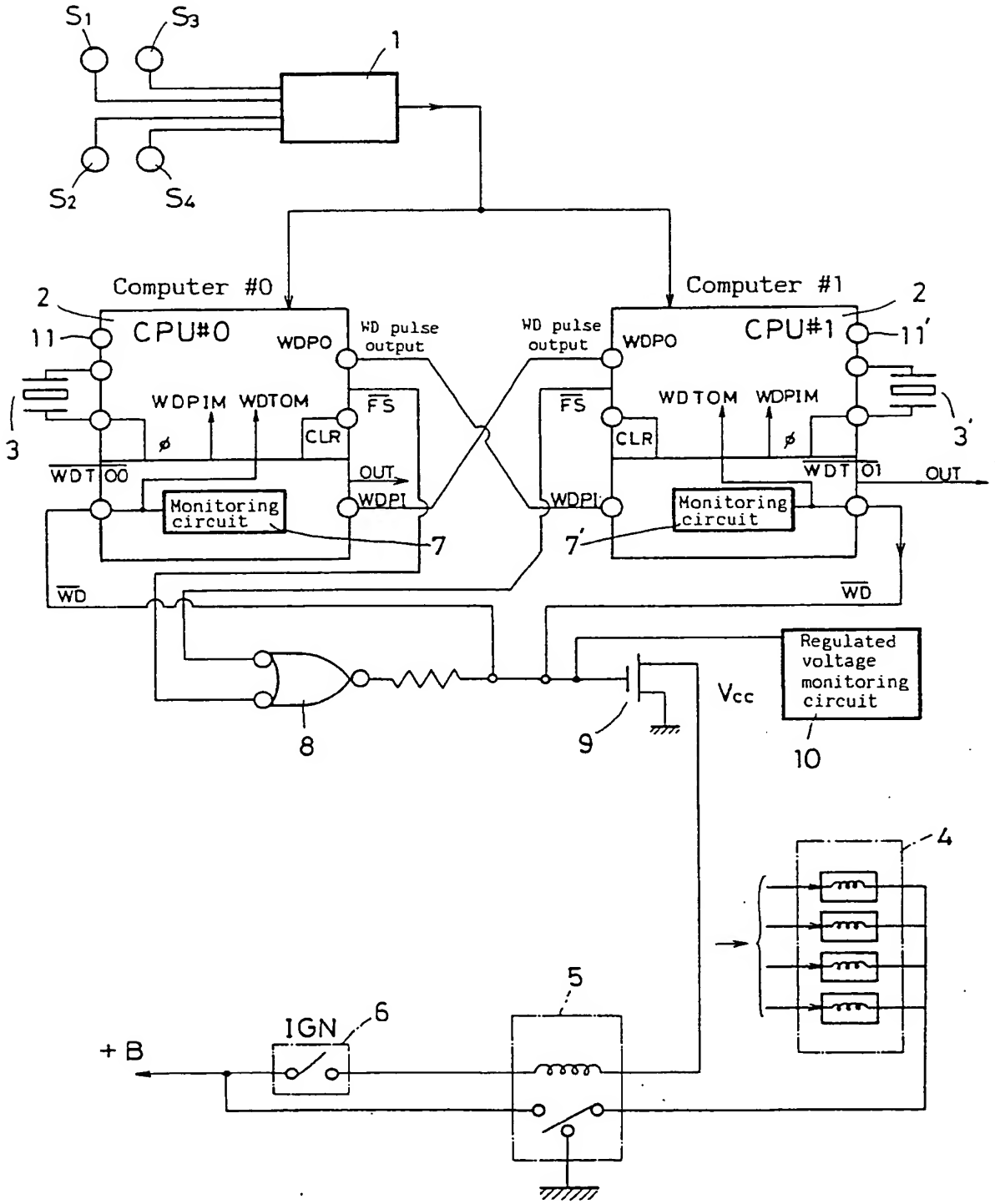
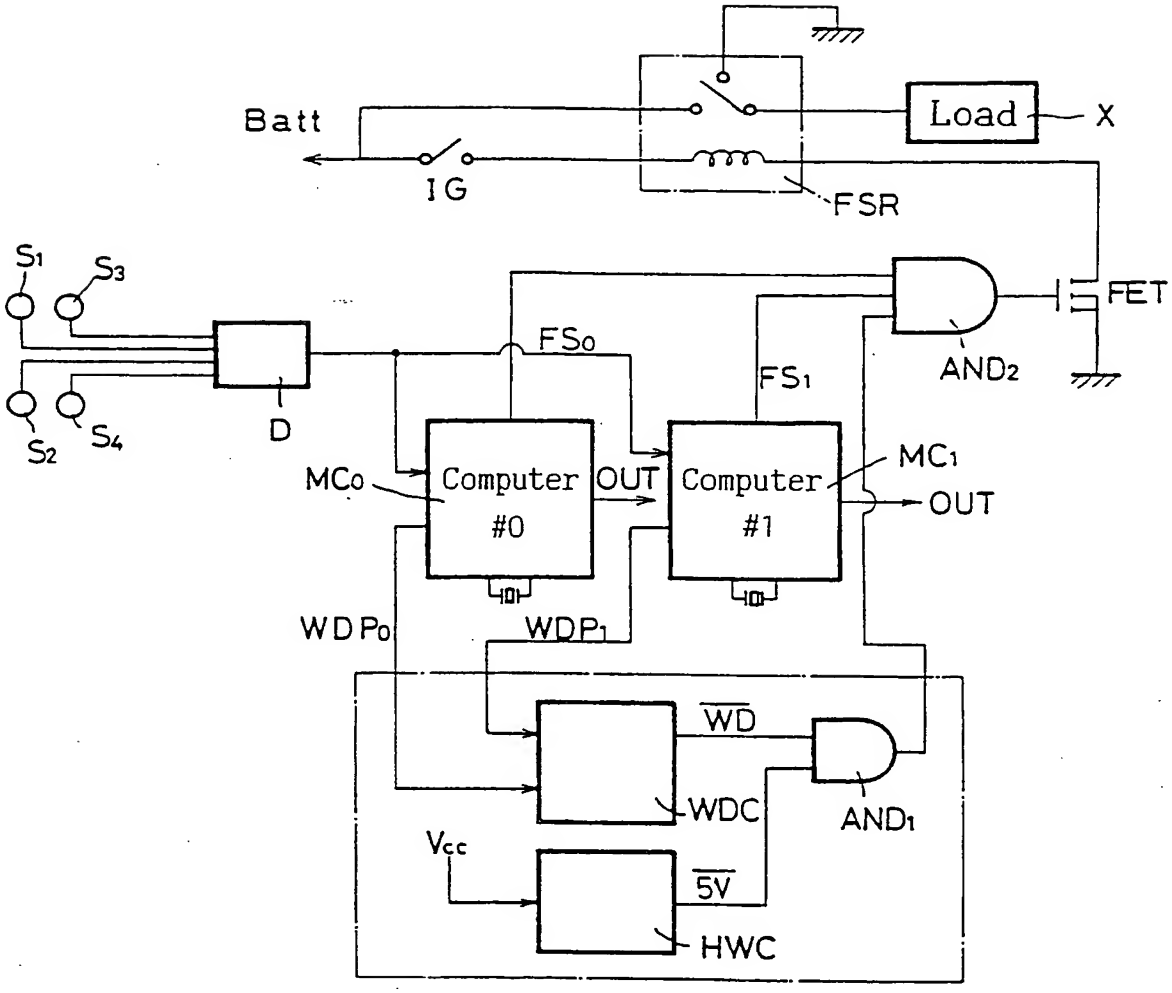

S1
S3
S2
S4
1
Computer #0
Computer #1
2
CPU#0
CPU#1
11
11'
WDPO
WD pulse output
WDPIM
WDTOM
FS
CLR
3
3'
WDT OO
WDT O1
OUT
WDPI
Monitoring circuit
7
7'
WD
8
9
Vcc
Regulated voltage monitoring circuit
10
4
5
IGN
6
+B

FIG. 2


Batt
IG
Load
X
FSR
S1
S3
S2
S4
D
FS0
FS1
AND2
FET
MC0
Computer #0
OUT
Computer #1
MC1
OUT
WDP0
WDP1
WD
WDC
AND1
Vcc
5V
HWC

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(88) Date of deferred publication of the search report:
13.04.94 Bulletin 94/15

(71) Applicant: Sumitomo Electric Industries, Ltd.
5-33, Kitahama 4-chome, Chuo-ku
Osaka 541(JP)

(72) Inventor: Hashiba, Hitoshi, c/o Osaka Works of Sumitomo
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Inventor: Ueda, Seiji, c/o Osaka Works of Sumitomo
Elec. Ind. Ltd
1-3, Shimaya 1-chome
Konohana-ku, Osaka(JP)

(74) Representative: Schieschke, Klaus, Dipl.-Ing.
Patentanwälte Dipl.-Ing. E. Eder
Dipl.-Ing. K. Schieschke
Elisabethstrasse 34
D-80796 München (DE)

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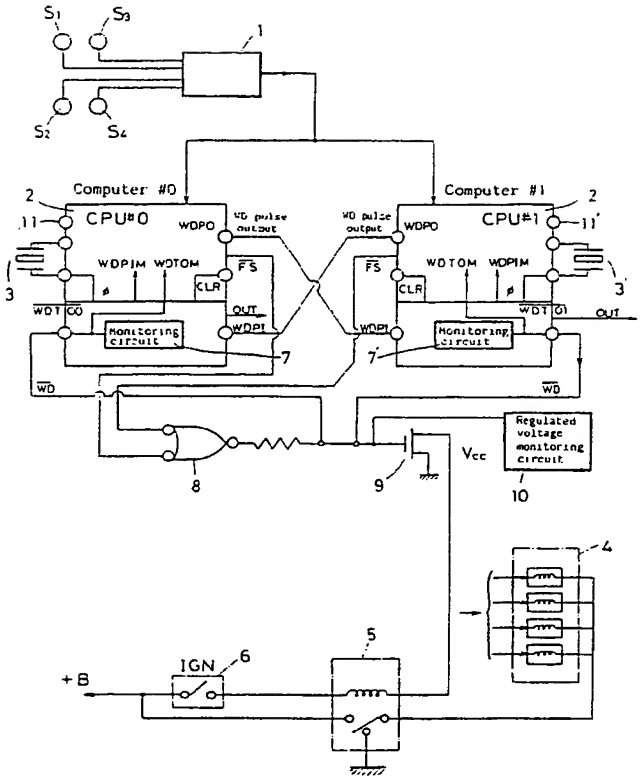
FIG. 1



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EUROPEAN SEARCH REPORT

Application Number
EP 93 10 9483

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.5)
Y	DE-A-37 26 489 (ROBERT BOSCH) * claim 1; figure 1 *	1-5	G05B23/02 G06F11/00
Y	EP-A-0 322 141 (LUCAS INDUSTRIES) * column 1, line 48 - column 4, line 37; figure 1 * * column 6, line 19 - column 6, line 40 * * column 8, line 42 - column 9, line 9 *	1-5	
A	DE-A-37 28 561 (VDO ADOLF SCHINDLING) * abstract *	6	
A	DE-A-37 00 986 (ROBERT BOSCH) * claim 1 *	1	
X	DE-A-21 08 836 (LICENTIA PATENT-VERWALTUNGS) * claim 1 *	1	
A	US-A-4 468 768 (SUNKLE ET AL) * abstract *	6	TECHNICAL FIELDS SEARCHED (Int.Cl.5)
A	WO-A-89 12272 (ROBERT BOSCH) * abstract *	4	G06F

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	14 February 1994	Guivol, Y

CATEGORY OF CITED DOCUMENTS

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